UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

PATENT NO. : 6,947,323 B2
APPLICATION NO. : 10/698752
DATED : September 20, 2005
INVENTOR(S) : Naso et al.



It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Line 51, delete "segments 416 and one or more protection registers 428 and" and insert --segments 416 and one or more protection registers 418 and--

Column 10, Line 12, delete "registers 428 and the associated lock bits are included as part " and insert --registers 418 and the associated lock bits are included as part --

Column 10, Line 15, delete "128 and lock bits to be accessed for read and write" and insert --418 and lock bits to be accessed for read and write--

Column 10, Line 18, delete "register 428 is maintained as a writeable/eraseable memory" and insert --register 418 is maintained as a writeable/eraseable memory --

Column 10, Line 22, delete "428 and its current data contents." and insert --418 and its current data contents.--

Column 10, Line 26, delete "lock bits of the protection registers 428. The bond pad of the" and insert --lock bits of the protection registers 418. The bond pad of the--

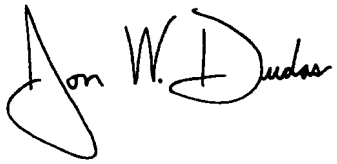
Column 10, Line 29, delete "This allows the protection registers 428 to be" and insert --This allows the protection registers 418 to be--

Column 10, Line 32, delete "and erase circuit 432 allows the protection registers 428 and" and insert --and erase circuit 432 allows the protection registers 418 and--

Column 10, Line 37, delete "verification testing of the protection registers 428 and" and insert --verification testing of the protection registers 418 and--

Signed and Sealed this

Fifth Day of June, 2007



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*Director of the United States Patent and Trademark Office*